IN THE CLAIMS

Claims 1-10 are canceled.

Cancel claims 11-27.

Claims 28-31 are canceled.

Cancel claim 32.

Claims 33-40 are canceled.

Cancel claims 41-64.

65. [New] A field emission display method comprising:

providing a monolithic semiconductive substrate;

providing an luminescent member spaced from and opposite the monolithic semiconductive substrate;

forming a plurality of emitter regions using the monolithic semiconductive substrates;

electrically isolating the plurality of emitter regions from one another;

providing a plurality of emitters within individual ones of the emitter regions;

providing a plurality of address circuits for respective ones of the emitter regions and individually comprising row circuitry and column circuitry;

coupling individual ones of the address circuits with emitters of respective individual ones of the emitter regions;

using the respective address circuits, providing an electrical potential across selected ones of the emitters of the respective emitter regions; and

responsive to the electrical potential, emitting electrons from the selected emitters towards the luminescent member to generate an image.

66. [New] The method of claim 65 wherein the providing the electrical potential comprises applying the electrical potential across different elevational portions of the selected emitters of the respective emitter regions.

67. [New] The method of claim 65 further comprising:

providing a vacuum intermediate the monolithic semiconductive substrate and the luminescent member; and

passing the electrons through the vacuum towards the luminescent member after the emitting.

68. [New] The method of claim 65 wherein the electrically isolating comprises etching the monolithic semiconductive substrate to define the emitter regions.

69. [New] The method of claim 65 wherein the providing the emitters comprises forming the plurality of emitters to comprise bulk substrate material of the monolithic semiconductive substrate.

70. [New] The method of claim 65 wherein the luminescent member comprises a face plate.

71. [New] The method of claim 65 wherein the luminescent member comprises a phosphor material configured to generate the image responsive to the reception of the electrons.

72. [New] The method of claim 65 wherein the address circuits are individually configured to address the emitters of individual ones of the respective emitter regions independent of others of the address circuits.

73. [New] The method of claim 65 wherein the providing the emitters comprises etching bulk semiconductive material of the monolithic semiconductive substrate.

74. [New] The method of claim 65 wherein the row circuitry and the column circuitry of an individual one of the address circuits comprise a plurality of address lines arranged orthogonal with respect to one another within the respective one of the emitter regions.

75. [New] The method of claim 65 wherein the coupling of the address circuits with the emitters of the respective emitter regions comprises configuring individual ones of the address circuits to address the emitters of the respective emitter region independent of addressing of the emitters of others of the emitter regions using others of the address circuits.

76. [New] A field emission device fabrication method comprising:

providing a monolithic semiconductive substrate;

defining a plurality of emitter regions using the monolithic semiconductive substrate;

forming a plurality of emitters within the emitter regions using the monolithic semiconductive substrate;

providing a plurality of drive signals configured to independently cause emission of electrons from the emitters of respective ones of the emitter regions;

electrically coupling the drive signals with the emitters of respective ones of the emitter regions and configured to cause the emission of electrons from the emitters of the respective ones of the emitter regions; and

providing a luminescent member arranged opposite to the emitters of the emitter regions and configured to receive the emitted electrons to generate an image.

77. [New] The method of claim 76 wherein the emitter regions are electrically isolated from one another.

78. [New] The method of claim 76 wherein the defining comprises etching the monolithic semiconductive substrate to electrically isolate the emitter regions.

79. [New] The method of claim 76 wherein the forming the emitters comprises etching bulk material of the monolithic semiconductive substrate.

80. [New] The method of claim 76 wherein the forming the emitters comprises forming the emitters to comprise bulk semiconductive material of the monolithic semiconductive substrate.

81. [New] The method of claim 76 wherein the forming the emitters comprises forming the emitters to comprise semiconductive material elevationally over the monolithic semiconductive substrate.

82. [New] The method of claim 76 wherein the forming the emitters comprises etching bulk semiconductive material of the monolithic semiconductive substrate.

83. [New] The method of claim 76 wherein the defining the emitter regions comprises electrically isolating the emitter regions.

84. [New] The method of claim 76 wherein the forming the emitters comprises electrically isolating the emitters of one of the emitter regions from the emitters of an other of the emitter regions.

85. [New] The method of claim 76 wherein the electrically coupling comprises coupling to apply the drive signals to different elevations of the emitters of the respective emitter regions.

86. [New] The method of claim 76 further comprising providing a vacuum intermediate the monolithic semiconductive substrate and the luminescent member and configured to pass the electrons towards the luminescent member.

87. [New] The method of claim 76 further comprising a plurality of drive circuits configured to provide the respective ones of the drive signals.

88. [New] The method of claim 76 wherein the providing the luminescent member comprises providing a face plate.

89. [New] The method of claim 88 wherein the forming the emitters comprises forming the emitters of a base plate, and further comprising spacing the face plate and the base plate using a plurality of spacers.

90. [New] A field emission base plate comprising:

a monolithic semiconductive substrate comprising bulk semiconductive substrate material; and

a plurality of emitter regions, wherein individual ones of the emitter regions comprise:

a plurality of emitters coupled with the monolithic semiconductive substrate; and

a first conductor and a second conductor positioned adjacent to the emitters of the respective emitter region at different elevations of the emitters and configured to apply an electrical potential to the emitters to cause emission of electrons from the emitters towards a face plate to form an image; and

address circuitry configured to provide a plurality of drive signals to the first conductor and the second conductor of respective ones of the emitter regions to

provide the electrical potential, and wherein the drive signals corresponding to one of the emitter regions differ from the drive signals corresponding to an other of the emitter regions.

91. [New] The plate of claim 90 wherein the emitter regions are electrically isolated from one another.

92. [New] The plate of claim 90 wherein the emitters of one of the emitter regions are electrically isolated from the emitters of an other of the emitter regions.

93. [New] The plate of claim 90 wherein the first conductor is positioned adjacent to tips of the emitters of the respective emitter region and the second conductor is positioned adjacent to bottoms of the emitters of the respective emitter region.

94. [New] The plate of claim 90 further comprising a plurality of spacers configured to space the base plate from the face plate.

95. [New] The plate of claim 90 wherein the monolithic semiconductive substrate comprises the bulk semiconductive substrate material of a wafer.

96. [New] The plate of claim 90 wherein the emitters comprise the bulk semiconductive substrate material.

97. [New] The plate of claim 90 wherein the address circuitry is configured to receive the different drive signals from the same common drive circuitry.

98. [New] The plate of claim 90 wherein the address circuitry is configured to receive the different drive signals from a plurality of drive circuits corresponding to respective ones of the emitter regions.

99. [New] The plate of claim 90 further comprising an electrically insulative layer configured to electrically insulate the first conductor from the second conductor.

100. [New] The plate of claim 90 further comprising a vacuum chamber elevationally above the emitters of the emitter regions.

101. [New] The plate of claim 90 wherein the address circuitry comprises a plurality of orthogonal rows and columns configured to provide the drive signals to respective ones of the emitter regions, wherein the drive signals for one of the emitter regions are independent of the drive signals for an other of the emitter regions.

102. [New] A field emission display device comprising:

a face plate comprising luminescent material configured to illuminate an image responsive to a plurality of electrons; and

a base plate formed using a monolithic semiconductive substrate and comprising:

a plurality of emitter regions which are individually electrically isolated from others of the emitter regions, wherein the emitter regions individually comprise:

a plurality of emitters configured to emit electrons towards the face plate, wherein the emitters of the individual respective emitter region are separately addressable from emitters of an other of the emitter regions; and

address circuitry configured to provide drive signals to the emitters of the respective emitter region to cause the emission of electrons towards the face plate; and

drive circuitry configured to provide different drive signals to the address circuitry of the different emitter regions to separately address the emitters of the respective ones of the emitter regions.

103. [New] The device of claim 102 wherein the emitter regions further comprise a first conductor positioned adjacent to tips of the emitters of the respective emitter region and a second conductor positioned adjacent to bottoms of the emitters of the respective emitter region.

104. [New] The device of claim 102 wherein the base plate further comprises an electrically insulative layer configured to electrically insulate the first conductor and the second conductor.

105. [New] The device of claim 102 further comprising a plurality of spacers configured to space the base plate from the face plate.

106. [New] The device of claim 102 further comprising a vacuum chamber intermediate the base plate and the face plate.

107. [New] The device of claim 102 wherein the monolithic semiconductive substrate comprises bulk semiconductive substrate material of a wafer.

108. [New] The device of claim 102 wherein the emitters comprise bulk semiconductive substrate material.

109. [New] The device of claim 102 wherein the drive circuitry comprises a plurality of drive circuits configured to provide the drive signals for respective ones of the emitter regions.

110. [New] The device of claim 102 wherein the address circuitry comprises a plurality of orthogonal rows and columns configured to provide the drive signals to the respective emitters.